

Computer Modeling of CAN Automotive Bus Transceivers

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Abstract

The paper describes models of an automotive bus transceiver that includes the effects of radio frequency interference on transmitter/receiver performance. Transceiver time-domain communication performance and radio frequency emissions are modeled and simulated using PSpice. These models have been experimentally verified in applications involving Controller Area Network (CAN) communication topologies such as those used in automobiles for real-time control.

Terms: Electromagnetic Interference (EMI), Controller Area Network (CAN), emissions, and radiation.

1. Introduction

In the past, modeling was carried out in order to verify the major operational functions of circuit and system components. The presence of interfering signals and signal emissions were not considered due to the relatively low packaging density of vehicle electronic equipment. However, the effects of radio frequency emissions have become more relevant recently, as the number of vehicle electronic devices has increased significantly. In fact, extraordinary expansion of vehicle control, navigation, and entertainment communication equipment has created new challenges in predicting electromagnetic radiation on communication data busses, whose major components are the bus transceivers. It is now desirable to evaluate EMI effects at the earliest possible stage of vehicle design.

Currently, the fastest communication data busses are composed of transceivers, twisted pair transmission lines, filters, and connectors. Models of these fast data buses can be developed based on circuit behavior in the presence of regular communication signals, as well as in the presence of special testing signals. (Of particular importance is the behavior of circuits in the presence of interfering signals.) Models such as these can help predict bus delays, signal reflection and integrity, and the effect of radio frequency emissions.

The following material provides the results of investigations related to the computer modeling of major hardware components of CAN automotive data busses, as for example, CAN transceivers, common mode filters, twisted pair, bus terminations, and ferrite-chip filters. Generic models of typical CAN vehicle network topologies were developed and experimentally verified to test bus delays, bus timing, signal integrity, bus tolerances, and conducted emissions.

2. Modeling and Testing the Bus Transceiver

The main focus of the modeling process was on high-speed CAN transceivers, such as the TJA 1050 from Philips. Transceiver modeling was a part of a larger project that included the following major steps:

1. Preparation of testing methods for transceivers and other components.
2. Tests of transceivers and other components.
3. Modeling of transceivers.
4. Modeling of filters.
5. Modeling of transmission lines.
6. Testing of simple communication links, such as two transceivers connected with a twisted pair.
7. EMC conducted emissions modeling.

Hardware and software tests of static and dynamic characteristics have been completed for the TJA 1050 CAN transceiver, whose performance is well known and easily comparable with the performance of older generation circuits. The following parameters have been identified for modeling:

1. Transmitter input thresholds to switch on and off the receiver.
2. Bus-to-receiver thresholds to switch on and off the receiver.
3. Transmitter and receiver voltage levels.
4. Dependence of different voltage levels and thresholds upon changes of the supply voltage.
5. Rise and fall times of the bus signals.
6. Rise and fall times of the receiver signal.
7. Transmitter-to-bus delay times.
8. Bus-to-receiver delay times.

Based on experimental data and specifications from the data sheet, a model of the TJA 1050 has been proposed and tested. Additional tests were performed to model common-mode chokes and ferrite chips applied in star the connectors of a Mercedes automobile. The simulation and measurement results are shown below. Simulation results indicate acceptable agreement with practical tests.

One of the most important ideas guiding modeling processes is broad application of generic PSPICE functional blocks, such as multipliers, integrators and differentiators. Figs 1 and 2 illustrate the general structure of a transceiver. Here, the transmitter and receiver models, including circuits simulating transceiver behavior, are described in terms of parameters 1 through 8 listed above. The circuits of Figs. 3, 6, and 7, together with their corresponding simulated waves, allow for the determination of most transceiver parameters. The simulated signals can be compared with the experimentally measured results shown in Figs. 9 and 10.

A circuit for testing conducted emissions is shown in Fig. 11, and its spectra is shown in Fig. 12. Conducted emissions are a major source of radiated emissions, which appear either due to asymmetry of the transceiver and other bus components, or due to ground or supply offset. These effects are illustrated in Figs. 13 and 14. The conducted emission levels simulated here agree with experimental test results included in [4]. Finally, a vehicle communication network with seven transceivers connected in a star configuration is shown in Fig. 15. The network also includes a star connector with ferrite filters to slow down the transitions on the bus line. The corresponding signals for the circuit are depicted in Fig. 16.

3. Conclusions

Simulation and test results of the time-domain communication and EMC parameters of the CAN bus transceivers have been presented. The simulations have been performed using the circuit simulator PSPICE, which allows for the combination of circuit level components with generic mathematical operational blocks. These types of PSpice models serve as valuable tools in investigating the behavior of complex automotive communication networks. This paper provides an example of the use of PSpice models in the investigation of network latencies, bus signal integrity, and conducted emissions.

Acknowledgements

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References

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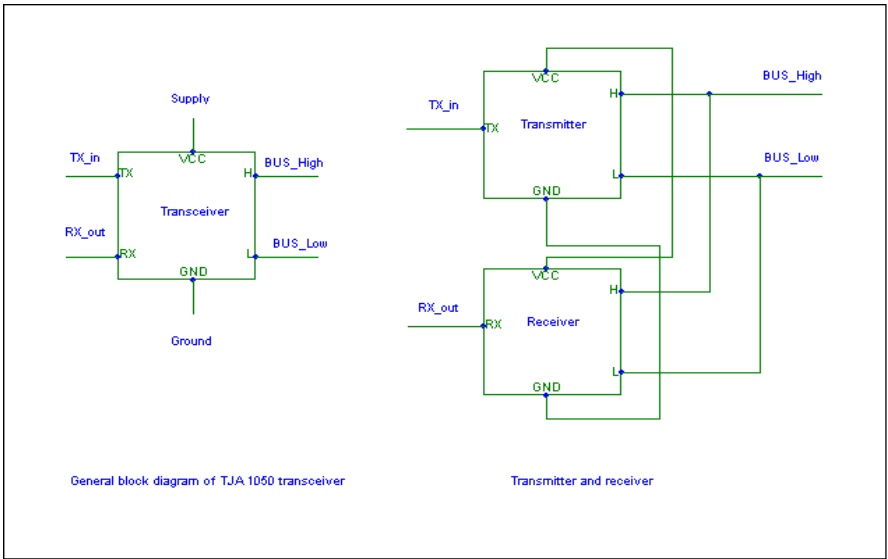


Fig. 1 General structure of a bus transceiver. Left diagram shows upper level block. Right diagram illustrates mid-level internal structure.

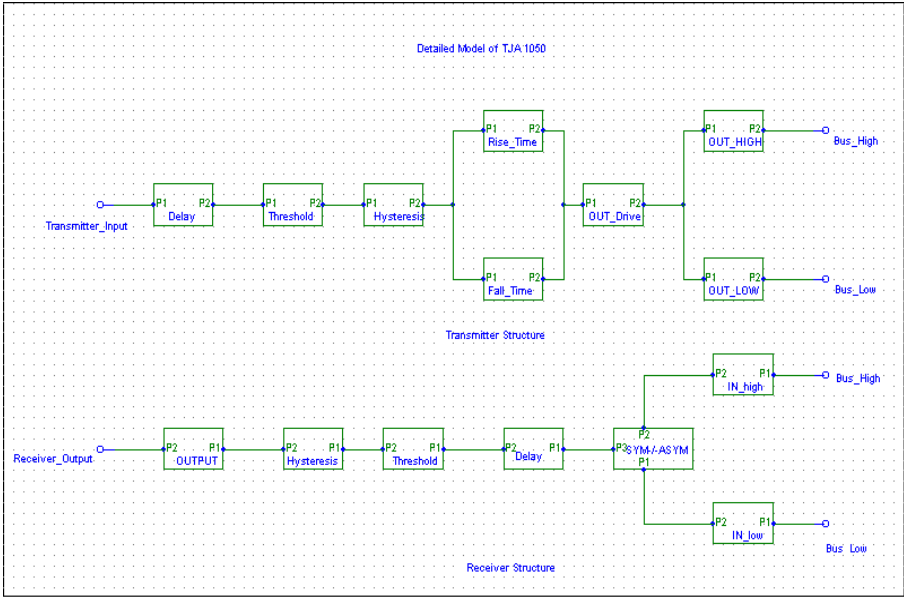


Fig. 2 Lower level internal blocks of the simulated transceiver. Upper diagram shows the transmitter, lower shows the receiver.

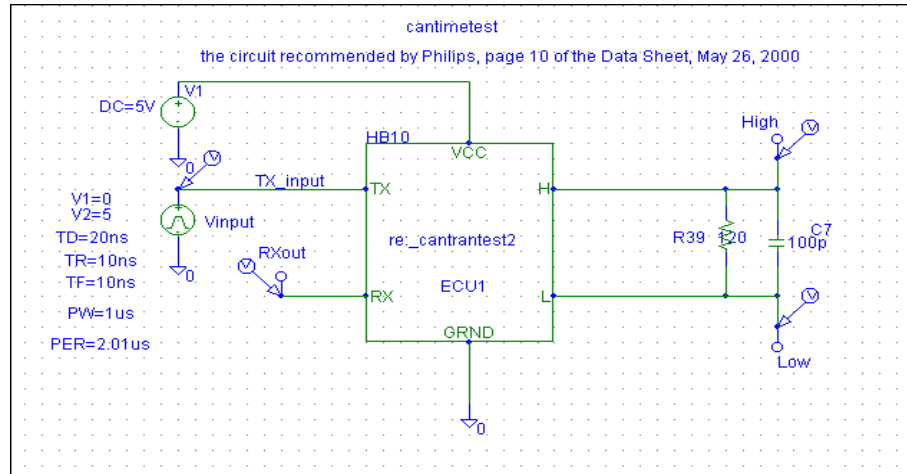


Fig. 3 Circuit to simulate time-domain behavior of the transceiver.

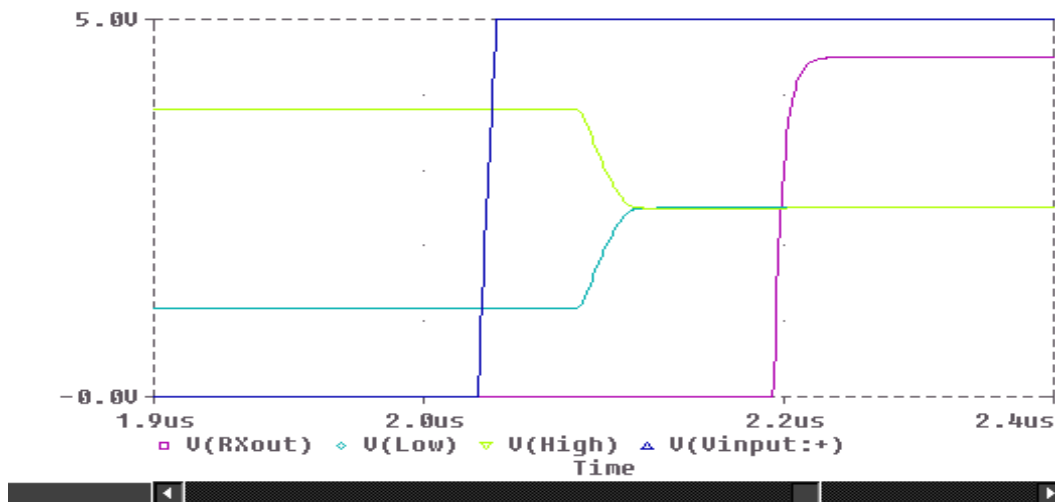


Fig. 4 Simulated time-domain waves of the transceiver. Left step shows a transmitter input step. Two symmetric transitions from dominant to recessive states are the bus signals. Rightmost step is the receiver delayed reaction.

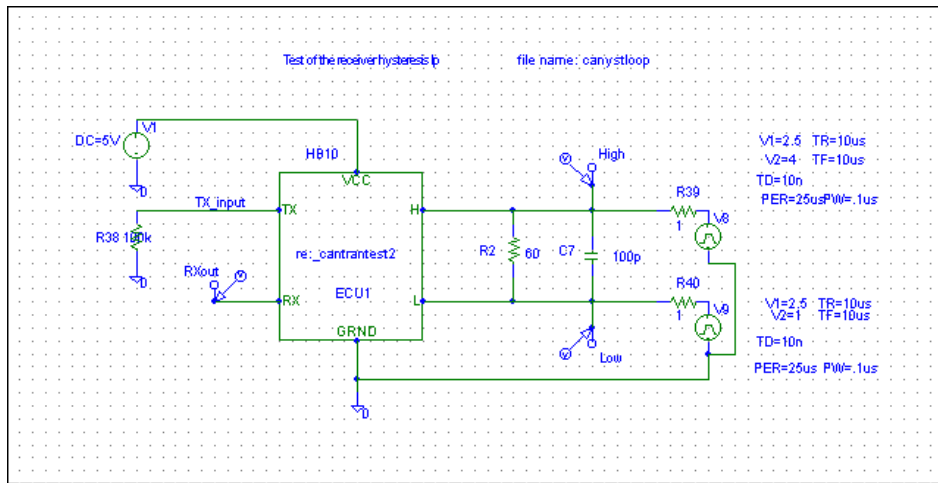


Fig. 5 Circuit to simulate receiver hysteresis.

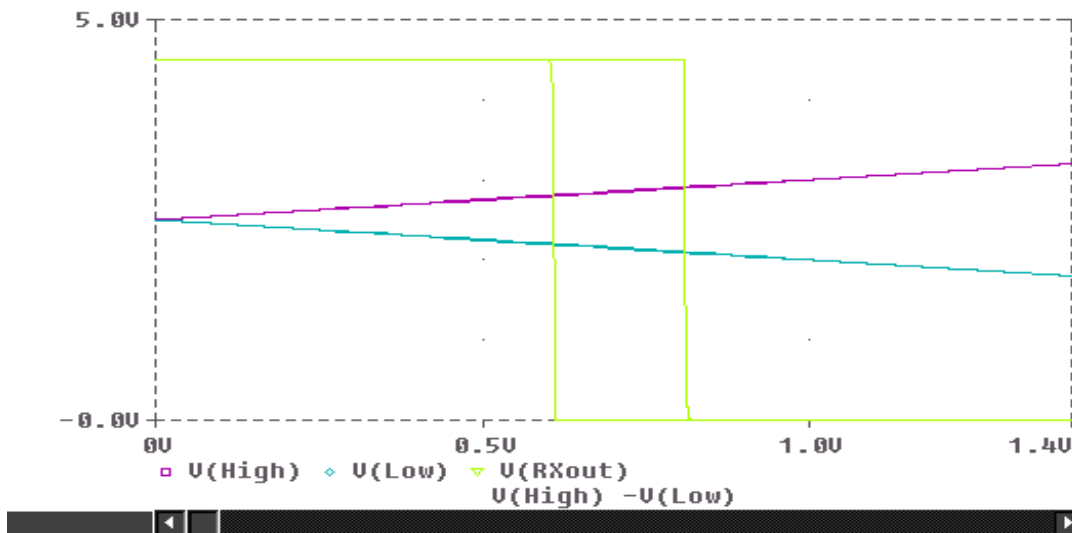


Fig. 6 Hysteresis loop of the receiver. Receiver output versus differential bus voltage is shown as the two steps, bus voltages are the two ramps.

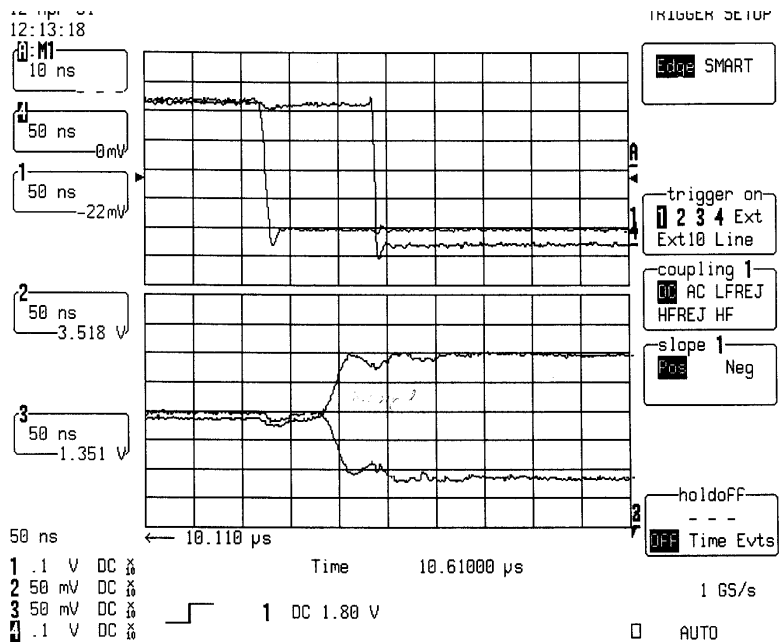


Fig. 9 Measured waves for the circuit of Fig. 7. Upper channel shows transceiver input signal (left), and receiver output signal. Lower channel shows recessive-to-dominant bus transitions.

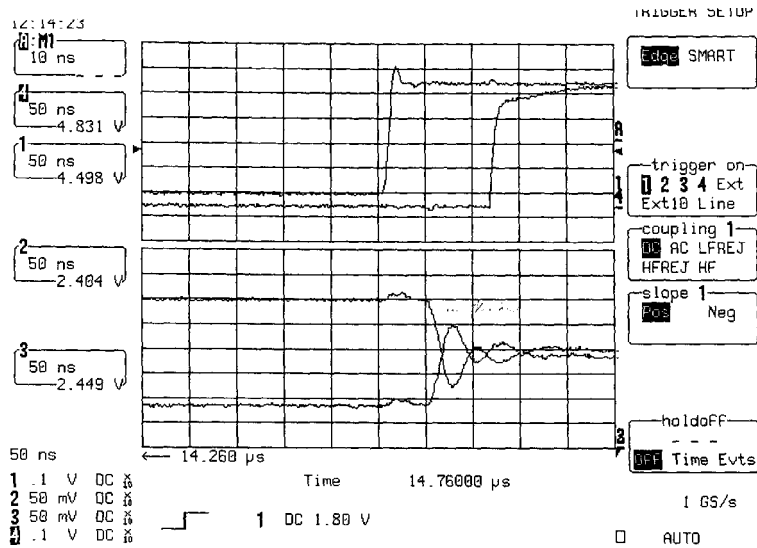


Fig. 10 Measured waves for the circuit of Fig. 7. Upper channel shows transceiver input signal (left), and receiver output signal. Lower channel shows dominant-to-recessive bus transitions.

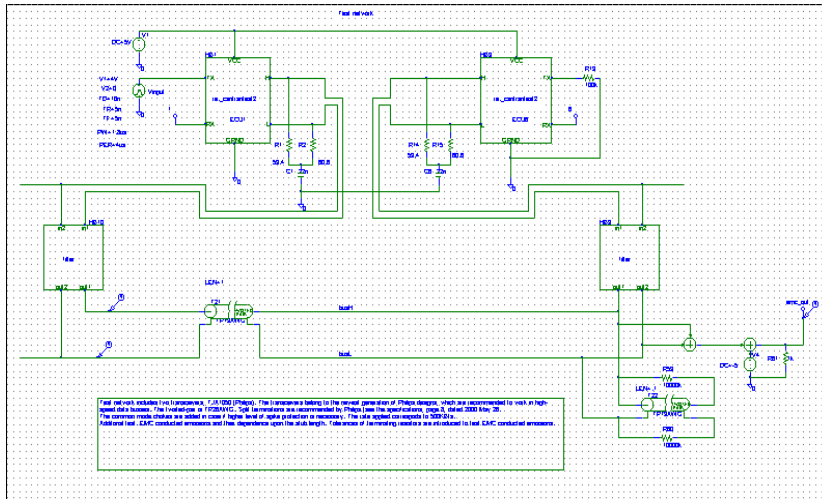


Fig. 11 Circuit for the simulation of bus conducted emissions effects.

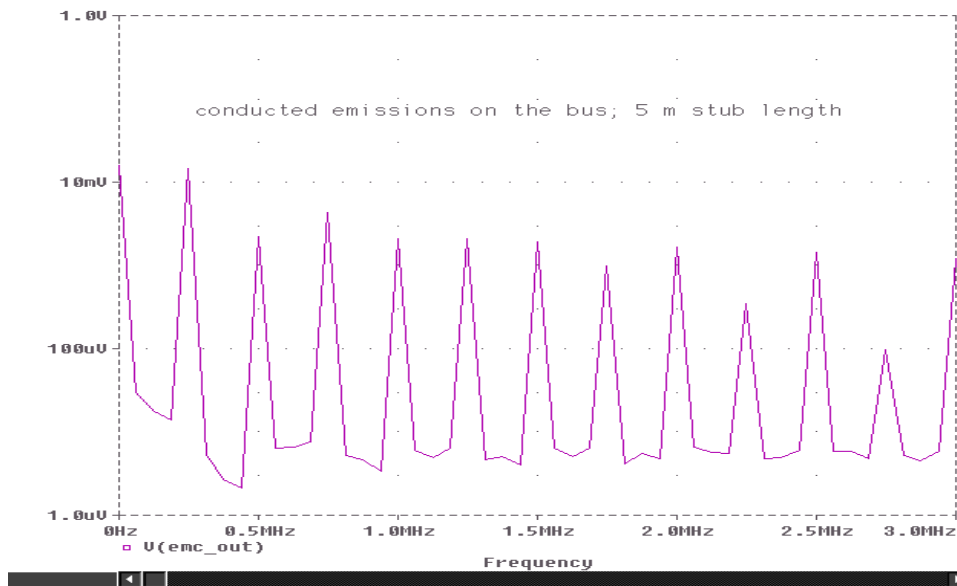


Fig. 12 Simulated conducted emissions due to resistor tolerances and insertion of an open stub.

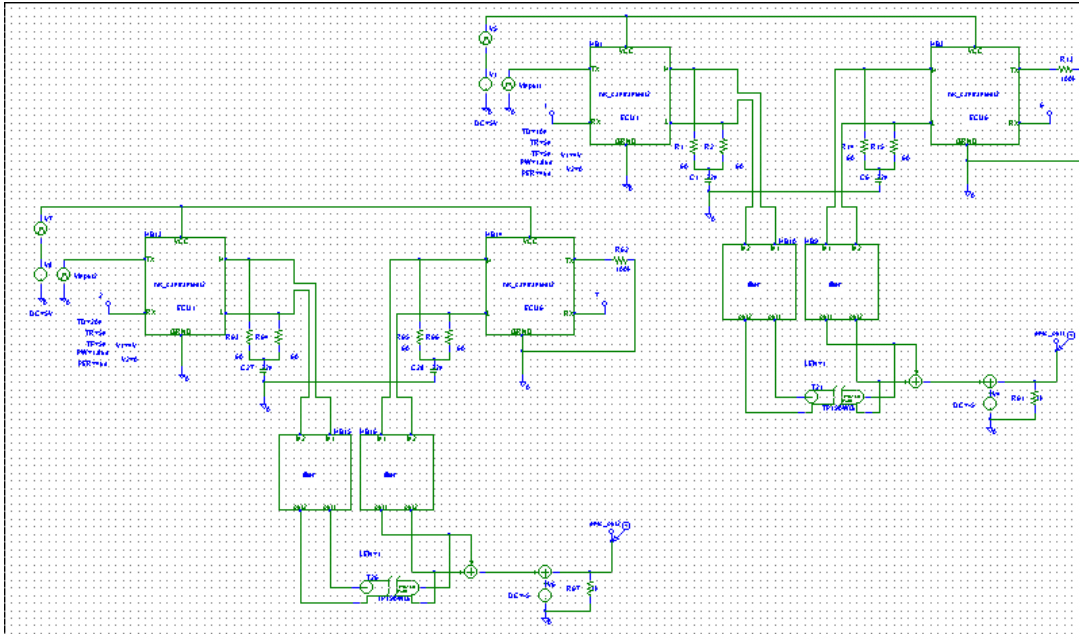


Fig. 13 Circuits applied to simulate effects of supply rail rejection factor on bus conducted emissions.

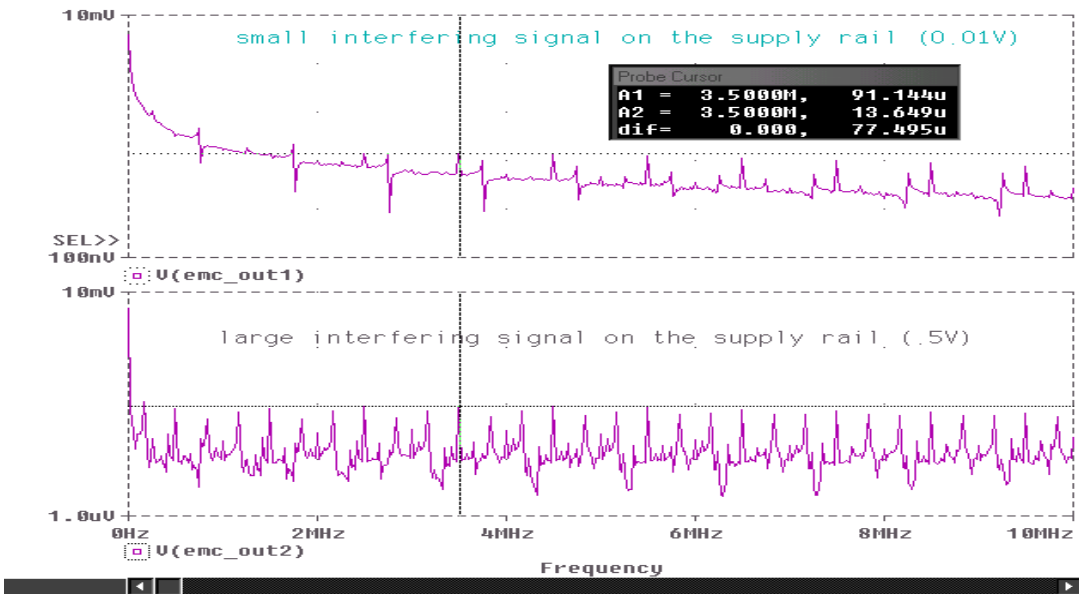


Fig. 14 Results of simulations for circuit of Fig. 13. Upper channel shows emission level when a small interfering signal is applied to the supply rail. Lower channel shows emission level for larger interfering signal applied to the supply rail.

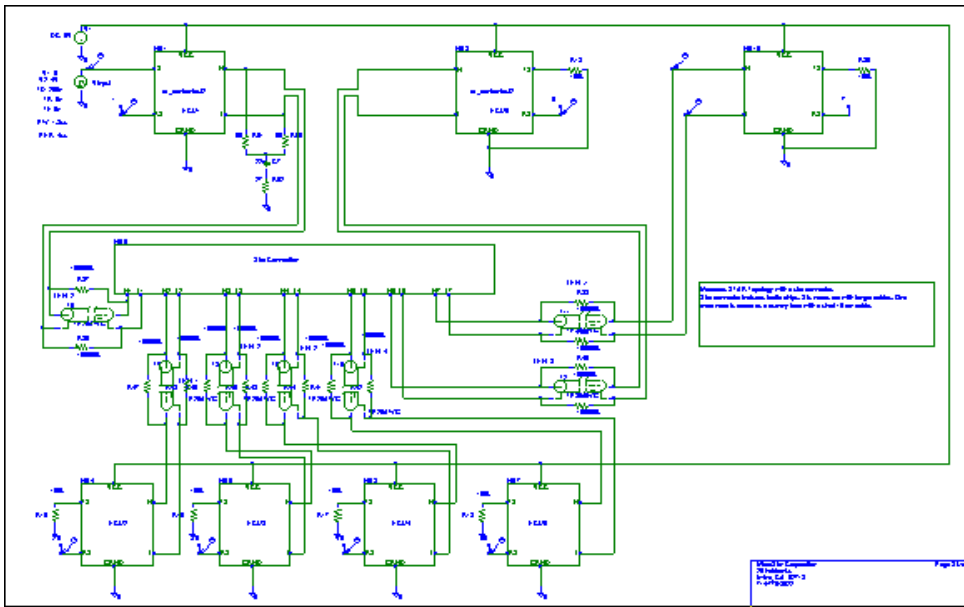


Fig. 15 Star topology with seven transceivers and a star connector with ferrite filters.

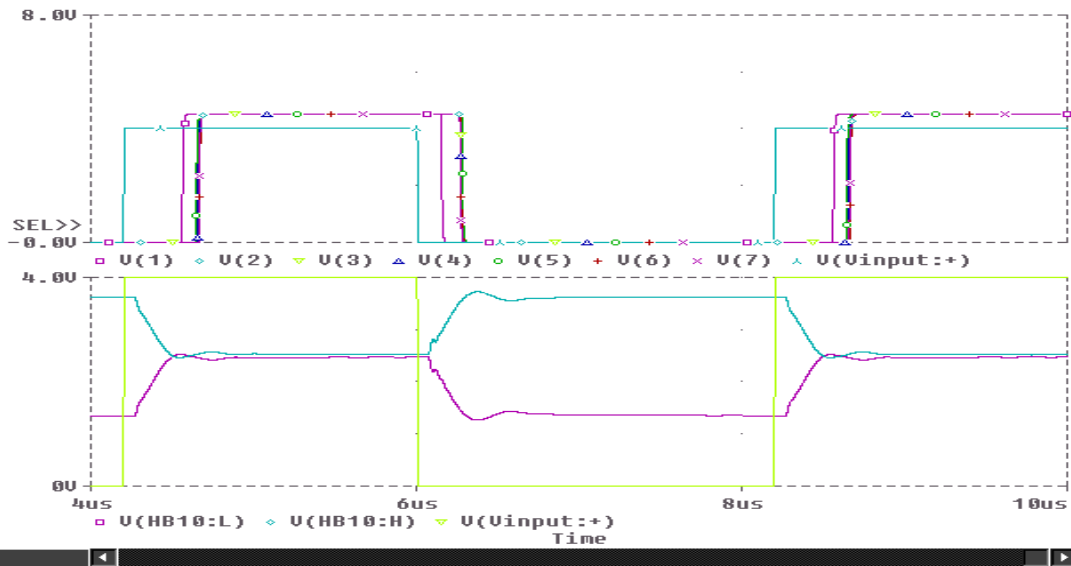


Fig. 16 Results of simulations of the topology of Fig. 15. Upper waves show the transmitter input signal (leftmost signal) and the receiver outputs. The lower signals (symmetric waves) are the bus voltages referenced to the transmitter input signal.